How Different Transistor Arrangements Impact Process Variability and Radiation Effects

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***Abstract*—This work evaluates the effects of process variability and radiation on a set of complex gates. These effects are compared to alternative circuits that implement the same functions but exploring basic cells as NAND2, NOR2 and Inverters with the goal of showing how the transistor arrangement impacts on the cell robustness. This paper adopts the 7nm FinFET ASAP High Performance at the electrical level. Results show that although complex cells present better timing and power results, circuits based on basic cells are up to 28% less sensible to radiation faults and about 40% more stable under process variability.**

***Index Terms*—process variability, radiation effects, complex gates, FinFET technology**

I. Introduction

Technology scaling increases the integration capacity of integrated circuits in a way that circuits have become increasingly dense and complex. New challenges were introduced in the design of integrated circuits due to scale down, such as increased manufacturing process variability, Short-Channel Effects (SCE), leakage current [1] and increased susceptibility to radiation effects. The focus of this work is to evaluate how process variability and the transient faults arising from the radiation effects impact circuits with a standard function, but with different transistor arrangements. A comparison is made between complex logic gates in their traditional versions and a multi-level of basic logic gates that implement the same function using NAND2, NOR2 and Inverter cells in FinFET technology.

Fin-Shaped Field Effect Transistor (FinFET) devices have vertical silicon structures to form the channel region and to connect the source and drain regions at each end [2]. The gate region is wrapped around this vertical structure, named as the fin. MOS channels are formed at the two sidewalls. The ON current (I_{ON}) of these devices is a function of the sum of the drive currents contributed by the two side-gate transistors. This fin-like geometry, where the depletion regions reach from the gates entirely into the body region, implies that no free charge carriers are available, making the suppression of SCE possible in FinFETs [3]. Fig. 1 presents FinFET key geometric parameters [4]: Gate length (L_G/L_{FIN}), fin height (H_{FIN}) and fin width/thickness (W_{FIN}/T_{SI}).

II. Methodology

This work evaluates the impact of process variability and radiation effects on different transistor arrangements.Three logic functions were chosen to perform this analysis: AOI22, OAI211 and XOR. Four different transistor arrangements are explored: Complex gate, only NAND2, only NOR2 and an NNI alternative, composed by NAND2, NOR2 and Inverter gates.

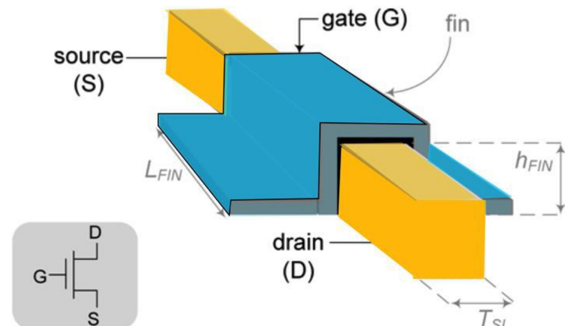

Fig. 1. Structure and geometric parameters of FinFETs [4].

On Complex gate transistor arrangement, the functions are optimized and designed as a complex logic gate CMOS topology. The functions are then converted, using De Morgan's theorem, into the three other transistor arrangements, in a way that only basic cells are employed. In Table I it is possible to observe the optimized function of each complex gate and its respective functions converted using only NAND2, only NOR2 and NNI.

Electrical simulations with the HSPICE tool were made using the 7nm FinFET technology from ASAP7 [5] to perform all the stages. Table II resumes the main parameter of the 7nm FinFET ASAP7 technology. In the circuits, the transistor sizing considers all transistors with three fins [6]. The nominal supply voltage is the ASAP7 model standard 0.7V. The minimum switching frequency of the input signals was 500MHz and four inverters (Fanout 4) were used as the load at the output of the circuit.

Nominal values are used as a form of reference values to evaluate the variability and radiation effects. The variability analysis considers the metal work function fluctuation (WFF) [7]. Metal gate work function exhibits a multi-nominal distribution, which can be approximated by a Gaussian distribution if the number of grains on the surface of metal-gate is high enough (>10). Thus, the WFF of each device is varied ac-

TABLE I
FUNCTIONS AND CORRESPONDING EQUATIONS ON THE TRANSISTOR ARRANGEMENTS EXPLORED

Topologia	XOR	OAI211	AOI22
Porta Complexa	Y = A.B' + A'.B	Y = (A+B . C.D)'	Y = (A.B + C.D)'
NAND2	Y = ((A . (B.B)')' . ((A.A)' . B)')'	Y = (((A.A)' . (B.B)')' . ((C.D)' . (C.D)')')'	Y = (((A.B)' . (C.D)')' . ((A.B)' . (C.D)')')'
NOR2	Y = ((((A+A)' + B)' + (A + (B+B)')')' + (((A+A)' + B)' + (A + (B+B)')')')'	Y = (((A+B)' + ((C+D)' + (C+D)')')' + ((A+B)' + ((C+D)' + (C+D)')')')'	Y = (((A+A)' + (B+B)')' + ((C+C)' + (D+D)')')'
NNI	Y = ((((A.B')')' + ((A'.B)')')')'	Y = ((((A'.B')')' + (C.D)')')'	Y = ((((A'+B')')' . (C+D)')')'

TABLE II
7NM FINFET ASAP7 MAIN PARAMETERS [5]

Parameter		7nm
Supply Voltage		0.7V
Gate Length (L_G)		21nm
Fin Width (W_{FIN})		6.5nm
Fin Height (H_{FIN})		32nm
Oxide Thickness (Tox)		2.1nm
Channel Doping		$1{\times}10^{22}m^{-3}$
Source/Drain Doping		$2{\times}10^{26}m^{-3}$
Work Function	**NFET**	4.3720eV
	PFET	4.8108eV

cording to a Gaussian distribution. Two thousand simulations were run for each logic gate [8]. The measurements were taken for a 3-sigma deviation of 3% of the WFF. Timing and power consumption measurements were made for each Monte Carlo simulation. Robustness analyzes were performed using the sigma/mean ratios of each delay arc, always aiming at the worst case.

The SET fault injection is modeled as the Messenger's equation shown in Eq. 1 [9], where Q_{coll} is the collected charge, τ_α ($1.64{\times}10^{-10}s$) is the collect charge timing constant, τ_β ($5{\times}10^{-11}s$) is the timing constant to establish the ion track and L (2μm) is the charge collection profundity [10].

$$I(t) = \frac{Qcoll}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}})$$
$$Qcoll = 10.8{\times}L{\times}LET \tag{1}$$

This effect is reproduced on the SPICE simulation as a current source, simulating the SET effects on the transistors. This work follows the parameter and methodology presented in [11], investigating the impact of SET 010 and 101 in all devices of the two inverters circuits. Thus, a current source is inserted into each internal node and the output of the circuit. Also, this evaluation considers all the input vectors for the selected logic gates. The simulation adopts a linear energy transfer (LET) of $1MeV - cm^2/mg$ and the fault is analyzed by observing the output voltage of the circuit. A fault is detected if the output of the circuit is bigger than $V_{DD}/2$ for logic level '0' and smaller than $V_{DD}/2$ for logic level '1'; otherwise, the fault was masked. The fault masking is determined by Eq. 2, considering the reason between the number of faults detected and the total faults inserted, i.e., a fault inserted in each internal node and the output, for each test vector of the circuit. For example, a logic gate with four inputs has 16 test vectors, if this same gate has five internal nodes plus the output, there would be 96 faults inserted in the circuit.

In the end, a general comparison of the results is also performed. The objective is to highlight which transistor arrangement presents the best results aiming only process variability and only transient faults, but also to give the arrangement that has an ideal average behavior in the three stages studied.

$$FaultMasking = \frac{FaultsDetected}{TotalFaultsInserted} \tag{2}$$

III. RESULTS

Complex gates reduce the number of literals in the equations and, consequently, this reflects on the fact that with this transistor arrangement, all the three functions evaluated presented better timing and power results. Fig. 2 compares the maximum transition time for all arches of each evaluated function. NAND2 versions of the circuits are about 18% slower than Complex gate versions, but NOR2 circuits could insert more than twice times of delay degradation on the OAI211.

The impact is even worse at the total power consumption on these experiments, i.e., during all the timing analysis. Fig. 3 shows that multi-level versions (NAND2, NOR2 and NNI) consumes at least 50% more on XOR cells (NAND2 version), and up to 129% on the AOI22 in NOR2 version than Complex gate circuits. Thus, to optimized circuits addressing power and timing reduction, the complex gate is the best alternative to transistor arrangement. Now, in sequence, the evaluation of the process variability and radiation effects will throw light on these effects on complex gates and the alternative circuits evaluated.

In general, complex gate circuits under process variability show the most significant variation in the delay compared to nominal behavior, reaching up to 5% on the worst case delay. Multi-level circuits presented a difference on the mean delay of 4%, 3% and 2% for NAND2, NOR2 and NNI alternative circuits. However, complex gate and NNI versions present mean power values statistically identical to the nominal power result, despite the large standard deviations. Table III shows the mean and standard deviation values obtained from the Monte Carlo simulation.

To compare the effects of process variability, considering both mean and standard deviation, are presented in Fig. 4 and

TABLE III
MEAN AND STANDARD DEVIATION RESULTS FOR POWER AND DELAY

Complex Gate	Measures	Complex		NAND2		NOR2		NAND2/NOR2/INV	
		Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma
XOR	Worst delay (ps)	17.1	3.1	19.7	1.9	28.2	3.6	21.5	1.9
	Power (nW)	213.8	9.8	311.8	15.6	401.3	17.8	394.6	23.2
AOI22	Worst delay (ps)	17.3	3.7	21.6	1.9	24.7	3.6	22.0	1.9
	Power (nW)	150.4	6.3	259.9	10.7	278.5	12.8	332.2	14.1
OAI211	Worst delay (ps)	16.5	2.8	19.1	2.1	34.2	4.1	22.4	1.9
	Power (nW)	153.3	6.5	281.1	13.2	363.8	17.5	264.9	13.9

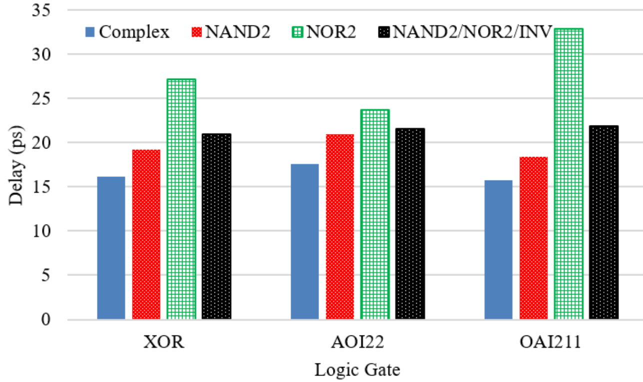

Fig. 2. Delay at nominal conditions.

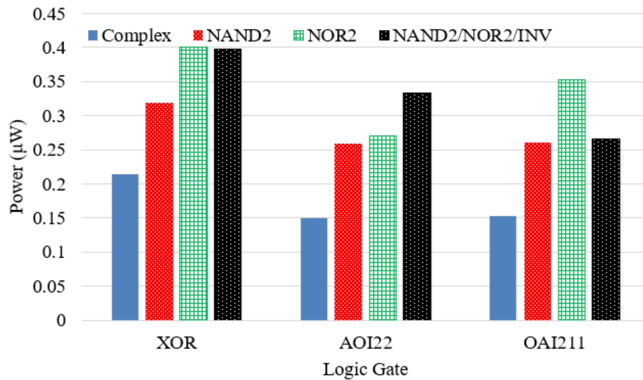

Fig. 3. Power at nominal conditions.

Fig. 5 respectively, the deviation results for delay and power. All the circuits demonstrate more sensibility on delay due to process variability than on power results. Complex gates significantly suffer the influence of process variability on delay. For all the three functions evaluated, this alternative shows the worst results with more than 15% of delay deviation. Multi-gate, with basic cells, alternatives demonstrate better delay robustness to process variability. NNI shows a slight advantage compared to NAND2 versions, with a difference of 1.5%. However, NAND2 versions present less power sensibility. One of the factors that contributes to the greater robustness of the multi-level topologies is the existence of identical elements in the vicinity, this guarantees an easy impression and final verification.

From the analysis of fault masking between the complex gate and the different arrangements with basic cells, the advantage of using basic cells is evident when the objective is to mitigate transient faults. In Fig. 6 this advantage can be noted mainly to arrangements that use only NAND2 and only NOR2 gates. For the XOR gate, the NAND2 and NOR2 arrangements present reductions of 7% and 14%, respectively, in the sensitivity to transient faults. For the AOI22 gate, this reduction is even more significant, being 18% for the arrangement with NAND2 and 28% for the arrangement with NOR2. The arrangement with NAND2 continues with the reduction of the sensitivity for the OAI211 gate (9%). However, the NOR2 arrangement has a small increase (1%) in the sensitivity for this case.

The arrangement using NAND2, NOR2 and Inverters to-

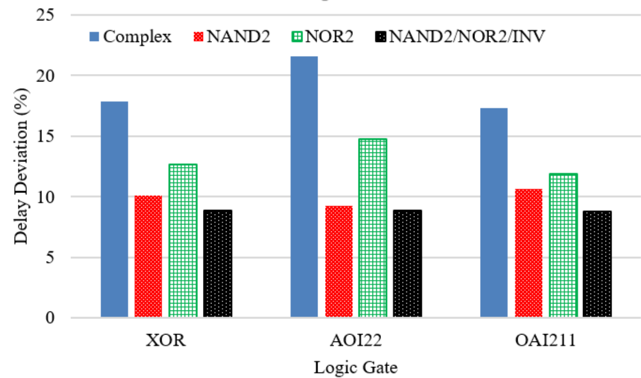

Fig. 4. Delay deviation due to process variability.

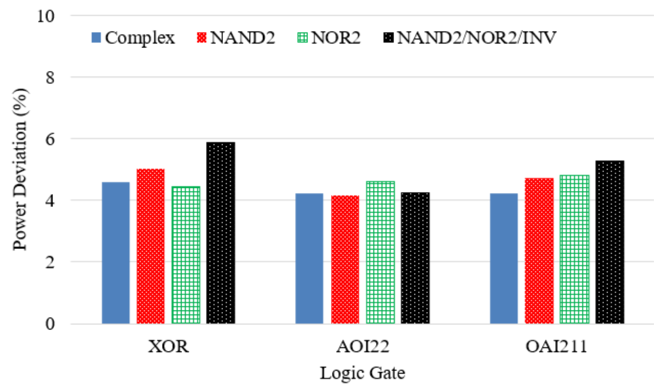

Fig. 5. Power deviation due to process variability.

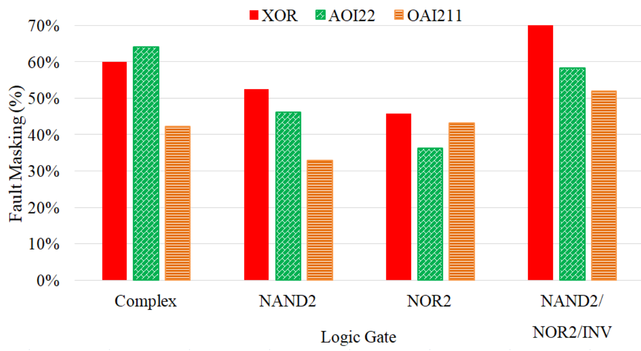

Fig. 6. Fault masking comparison.

gether does not perform well about the fault masking. Only for the AOI22 gate, this arrangement has a sensitivity reduction (6%), whereas for the XOR and OAI211 gates there is a 10% increase in sensitivity. Although the NOR2 arrangement presents the highest percentages of sensitivity reduction to transient faults, the NAND2 arrangement is the most stable, having a significant reduction for all three gates used in this study. Tables IV, V and VI show the total of faults injected in each logic function analyzed. Moreover, the number of faults masked and detected also are showed.

TABLE IV
FAULT ANALYSIS OF XOR GATE

Fault Analysis/ Topologies	XOR			
	Complex	NAND2	NOR2	NAND2/ NOR2/INV
Inserted	20	40	48	44
Detected	12	21	22	31
Masked	8	19	26	13
Fault Masking	**60.0%**	**52.5%**	**45.8%**	**70.5%**

TABLE V
FAULT ANALYSIS OF OAI211 GATE

Fault analysis/ Topologies	OAI211			
	Complex	NAND2	NOR2	NAND2/ NOR2/INV
Inserted	64	192	192	160
Detected	27	63	83	83
Masked	37	129	109	77
Fault Masking	**42.2%**	**32.8%**	**43.2%**	**51.9%**

TABLE VI
FAULT ANALYSIS OF AOI22 GATE

Fault Analysis/ Topologies	AOI22			
	Complex	NAND2	NOR2	NAND2/ NOR2/INV
Inserted	64	128	224	208
Detected	41	59	81	121
Masked	23	69	143	87
Fault Masking	**64.1%**	**46.1%**	**36.2%**	**58.2%**

IV. CONCLUSIONS

This work presented an evaluation of how the transistor arrangement influences the cell robustness against process variability and the radiation effects on 7nm FinFET ASAP technology. At nominal conditions, complex gate arrangement is the best alternative to obtain less power consumption and a decrease in the propagation delay. It occurs because the complex gate arrangement reduces the number of transistors and the connections between them significantly. However, when the behavior of the logic gates is investigated with radiation or process variability effects, the multi-level arrangements are the best option. Compared to multi-level of basic cells topologies, complex gates delay deviation impact over 30% of the stability of the functions. Finally, under the impact of radiation or process variations, better results can be found using the topologies based on multi-level arrangements. Aiming at future work, more in-depth analyzes will be carried out regarding the effects of radiation. Also, the impact of the transistors sizing on these effects will also be analyzed.

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